IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

YERVANT ZORIAN

Application No.: 10/083,241

Filed: February 25, 2002

For: **Apparatus and Method to Generate a Repair Signature**

Art Group: 2133

Examiner: Ton, David

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Request for Continued Examination. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10-3-05

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

10-03-05

Deborah A. McGovern *Date*

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	10/083,241
Filing Date	February 25, 2002
First Named Inventor	Yervant Zorian
Art Unit	2133
Examiner Name	Ton, David
Attorney Docket Number	4640P006

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] *(if known)*	Publication Date or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,181,614	01-30-2001	Aipperspach et al.	
		US-6,304,989	10-16-2001	Kraus et al.	
		US-6,408,401	06-18-2002	Bhavsar et al.	
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		US-6,396,760	05-28-2002	Behera et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 08/11/2003.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet	2	of	2

Complete if Known	
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First Named Inventor	Yervant Zorian
Art Unit	2133
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Attorney Docket Number	4640P006

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		TSIN-YUANCHANG et al., "Tutorial 2: SoC Testing and P1500 Standard", Asian Test Symposium 2000: 492	
		ERIK JAN MARINISSEN et al., "Wrapper Design for Embedded Core Test", ITC 2000: 911-920.	
		ALFREDO BENSO et al., "HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SOCS", ITC 1999: 1038-1044	
		D. GIZOPOULOS et al, "Low Power/Energy BIST Scheme for Datapaths", VTS 2000: pp. 6 total.	
		V.A. VARDANIAN et al., "A March-based Fault Location Algorithm for Static Random Access Memories", MDTD 2002: 256-261 July 10-12, 2002	
		ALFREDO BENSO et al., "HD2BIST: a Hierarchical Framework for BIST Scheduling, Data patterns delivering and diagnosis in SoCs", ITC 2000: pp. 10 total.	
		YERVANT ZORIAN et al., "Embedded-Memory Test and Repair: Infrastructure IP for SoC Yield", IEEE CS and IEEE CASS May-June 2003: 58-66	
		YERVANT ZORIAN et al., "Embedding Infrastructure IP for SoC Yield Improvement", June 2002, pp. 709-712.	
		PRAVEEN PARVATHALA et al., "FRITS-A Microprocessor Functional BIST Method", March 2002, pp. 590-598	

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